Amendments to the Claims

A complete set of the existing claims are set forth below, with the amended claims showing deletions (strikethroughs) and insertions (underline).

1 -33. (Cancelled)

34. (Original) An apparatus for inserting one or more data bytes into a stream of data words, comprising:

a first circuit to generate a plurality of multi-bit data bit selection masks; and

a second circuit coupled to said first circuit to generate an output data word conditionally using selected parts of a first and a second intermediate data word generated from a first input data word of a current cycle, a third and a fourth intermediate data word generated from a second input data word of a preceding cycle, a first re-aligned variant of a first insertion data word of the current cycle, and a second re-aligned variant of a second insertion data word of the preceding cycle, in accordance with said data bit selection masks.

35. – 36. (Cancelled)

37. (Original) The apparatus of claim 34, wherein said first circuitry comprises a plurality of shifters, a first plurality of logical operators correspondingly coupled to selected ones of said shifters, and a second plurality of logical operators correspondingly coupled to selected ones of said first logical operators for generating said multi-bit data bit selection masks.

38. (Original) The apparatus of claim 34, wherein the apparatus is a selected one of an application specific integrated circuit, a micro-controller, a digital signal processor, a general purpose microprocessor, and a network processor.